IN THE CLAIMS

Please amend claim 10 and add new claims 12-27 as follows:

Claim 1 (Previously Presented): A high power semiconductor device for a radio communication system, comprising:

a compound semiconductor substrate having a resistivity less than 1.0×10^8 Ohm-cm at least at surface thereof;

a buffer layer formed on the compound semiconductor substrate and having a super lattice structure; and

an active layer formed on the buffer layer and having a high power active element for radio communication formed therein.

Claim 2 (Previously Presented): The semiconductor device as claimed in claim 1, wherein the compound semiconductor substrate has a resistivity less than 0.6×10^8 Ohm-cm.

Claim 3 (Previously Presented): The semiconductor device as claimed in claim 1, wherein the active layer is formed at a position within 5.0 μm from the surface of the compound semiconductor substrate.

Claim 4 (Previously Presented): The semiconductor device as claimed in claim 1, further comprising an electrode layer formed on another surface of the compound semiconductor substrate.

Claim 5 (Previously Presented): The semiconductor device as claimed in claim 4, wherein the electrode layer is not electrically connected to any power supply potential of the semiconductor device.

Claim 6 (Previously Presented): The semiconductor device as claimed in claim 4, wherein the electrode layer is connected to one power supply potential of the semiconductor device.

Claim 7 (Previously Presented): The semiconductor device as claimed in claim 1, further comprising:

a source electrode and a drain electrode formed on the active layer, separated from each other so as to establish a channel region, and

a gate electrode formed above the channel region.

Claim 8 (Previously Presented): The semiconductor device as claimed in claim 7, wherein the active layer has 2-Dimensional Electron Gasses.

Claim 9 (Previously Presented): The semiconductor device as claimed in claim 1, wherein the active layer comprises:

a collector layer of a first conducting type;

a base layer of a second conducting type formed on the collector layer;

an emitter layer of the first conducting type formed on the base layer.

Claim 10 (Currently Amended): A high power semiconductor device for a radio communication system, comprising:

a compound semiconductor substrate having a resistivity less than 1.0×10^8 Ohm-cm at least at surface thereof;

a buffer layer formed on the compound semiconductor substrate and having a super lattice structure; and

an active layer formed on the buffer layer and having ~~an~~ a high power active element formed therein,

wherein the compound semiconductor substrate has a resistivity more than 1.0×10^8 Ohm-cm in total.

Claim 11 (Canceled).

Claim 12 (New): The semiconductor device as claimed in claim 1, wherein the buffer layer has a GaAs/A1GaAs supper lattice structure.

Claim 13 (New): The semiconductor device as claimed in claim 1, wherein the

GaAs/A1GaAs super lattice structure includes undoped GaAs layers having a carrier concentration less than 1 x 10^5 cm^{-3}.

Claim 14 (New): The semiconductor device as claims in claim 12, wherein the GaAs/A1GaAs super lattice structure includes unhoped A1GaAs layers have a carrier concentration less than 1 x 10^{16} cm^{-3}.

Claim 15 (New): The semiconductor device as claimed in claim 1, wherein the active layer is doped with Si to a concentration of 1 x 10^{17} cm^{-3}.

Claim 16 (New): The semiconductor device as claimed in claim 1, wherein the compound semiconductor device substrate is a GaAs substrate.

Claim 17 (New): The semiconductor device as claimed in claim 1, wherein the super lattice buffer layer is disposed between the compound semiconductor substrate and the active layer such that, when the semiconductor device is activated, the super lattice buffer layer inhibits electrical field concentration in the active layer.

Claim 18 (New): The semiconductor device as claimed in claim 1, wherein the super lattice buffer layer is disposed between the compound semiconductor substrate and the active layer such

that, when the semiconductor device is activated, the super lattice buffer layer inhibits electrons leaking from the active layer from accumulating at the interface between the low-resistance substrate and the buffer layer.

Claim 19 (New): The semiconductor device as claimed in claim 1, wherein the super lattice buffer layer is disposed between the compound semiconductor substrate and the active layer such that, when the semiconductor device is activated, the super lattice buffer layer inhibits domain generation in the buffer layer under high power operating conditions.

Claim 20 (New): The semiconductor device as claimed in claim 10, wherein the buffer layer has a GaAs/A1GaAs super lattice structure.

Claim 21 (New): The semiconductor device as claimed in claim 20, wherein the GaAs/A1GaAs super lattice structure includes undoped GaAs layers having a carrier concentration less than $1 \times 10^{15}\ cm^{-3}$.

Claim 22 (New): The semiconductor device as claims in claim 20, wherein the GaAs/A1GaAs super lattice structure includes undoped A1GaAs layers having a carrier concentration less than $1 \times 10^{16}\ cm^{-3}$.

Claim 23 (New): The semiconductor device as claimed in claim 10, wherein the active layer is doped with Si to a concentration of $1 \times 10^{17}\ cm^{-3}$.

Claim 24 (New): The semiconductor device as claimed in claim 10, wherein the compound semiconductor device substrate is a GaAs substrate.

Claim 25 (New): The semiconductor device as claimed in claim 10, wherein the super lattice buffer layer is disposed between the compound semiconductor substrate and the active layer such that, when the semiconductor device is activated, the super lattice buffer layer inhibits electrical field concentration in the active layer.

Claim 26 (New): The semiconductor device as claimed in claim 10, wherein the super lattice buffer layer is disposed between the compound semiconductor substrate and the active layer such that, when the semiconductor device is activated, the supper lattice buffer layer inhibits electrons leaking from the active layer from accumulating at the interface between the low-resistance substrate and the buffer layer.

Claim 27 (New): The semiconductor device as claimed in claim 10, wherein the super buffer layer is disposed between the compound semiconductor substrate and the active layer such that, when the semiconductor device is activated, the super lattice buffer layer inhibits domain generation in the buffer layer under high power operating conditions.